CLAIMS

What is claimed is:

1. A method for updating an adaptive algorithm for processing data, comprising the steps of:
   a) processing a data sequence in accordance with the adaptive algorithm to produce a processed data sequence;
   b) filtering the data sequence with a first set of filter characteristics to generate a filtered data term for the adaptive algorithm;
   c) generating a filtered error term for the adaptive algorithm from at least the processed data sequence using a second set of filter characteristics, said second set of filter characteristics being similar to said first set of filter characteristics; and
   d) updating the adaptive algorithm in response to said filtered data term and said filtered error term.

2. The method of Claim 1, wherein said generating step c) comprises convolving the processed data sequence with said second set of filter characteristics to generate a filtered processed data sequence.

3. The method of Claim 2, wherein said generating step c) further comprises determining a difference between the filtered processed data sequence and an ideal filtered processed data sequence to produce said filtered error term.

4. The method of Claim 3, further comprising (i) detecting a sequence of said processed data sequence, and (ii) convolving said detected processed data sequence with a third set of filter characteristics to generate said ideal filtered processed data sequence.

5. The method of Claim 4, wherein said first set of filter characteristics is identical to said second set of filter characteristics.

6. The method of Claim 4, said third set of filter characteristics comprising a subset of filter characteristics similar or identical to said first and second sets of filter charactieristics.

7. The method of Claim 1, wherein said generating step c) comprises determining a difference between the processed data sequence and an ideal processed data sequence to produce an error term.

8. The method of Claim 7, wherein said generating step c) further comprises convolving the error term with said second set of filter characteristics to generate said filtered error term.

9. The method of Claim 7, further comprising (i) further processing said processed data sequence with a sequence detector, and (ii) convolving said sequence-detected processed data sequence with a third set of filter characteristics to generate said ideal filtered processed data sequence.

10. The method of Claim 1, wherein each of said first and second sets of filter characteristics comprises an error filter.

11. The method of Claim 10, wherein said filtering further comprises transposing a channel response to generate at least a subset of said first set of filter characteristics.

12. The method of Claim 1, wherein said data sequence comprises a digital data signal.

13. The method of Claim 1, wherein said processing step a) comprises equalizing said data sequence, said processed data sequence comprises an equalized data signal, said filtered processed data sequence comprises a filtered equalized data signal, and said ideal filtered processed data sequence comprises an ideal filtered equalized data signal.

14. The method of Claim 1, wherein said first and second sets of filter characteristics are configured to minimize a dominant error type.

15. The method of Claim 14, wherein said dominant error type comprises a single bit error.

16. The method of Claim 15, wherein said first and second sets of filter characteristics are further configured to minimize a dibit error.

17. A computer-readable medium or waveform containing a set of instructions which, when executed by a signal processing device configured to execute computer-readable instructions, is configured to perform the method of claim 1.

18. The computer-readable medium or waveform of Claim 17, wherein said adaptive algorithm comprises an adaptive finite impulse response (FIR) algorithm.

19. The computer-readable medium or waveform of Claim 18, wherein said adaptive FIR algorithm comprises a least-mean-squares (LMS) gradient algorithm.

20. The computer-readable medium or waveform of Claim 17, wherein said processing step a) comprises equalizing said data sequence.

21. The computer-readable medium or waveform of Claim 17, wherein said generating step c) comprises (i) detecting a sequence of said processed data sequence, and (ii) convolving said sequence-detected, processed data sequence with said second set of filter characteristics to generate a filtered processed data sequence.

22. The computer-readable medium or waveform of Claim 21, wherein said generating step c) further comprises subtracting an ideal filtered processed data sequence from the filtered processed data sequence to generate said filtered error term.

23. The computer-readable medium or waveform of Claim 17, wherein said generating step c) comprises subtracting an ideal processed data signal from the processed data signal to generate an error term.

24. The computer-readable medium or waveform of Claim 23, wherein said generating step c) further comprises convolving said error term with said second set of filter characteristics.

25. The computer-readable medium or waveform of Claim 17, wherein each of said first and second sets of filter characteristics comprises an error filter.

26. The computer-readable medium or waveform of Claim 17, wherein said method further comprises minimizing a dominant error type.

27. The computer-readable medium or waveform of Claim 26, wherein said dominant error type comprises a single bit error.

28. The computer-readable medium or waveform of claim 17, wherein said set of instructions comprises object code, source code and/or binary code.

29. The computer-readable medium or waveform of claim 17, wherein said set of instructions comprises digital code configured for processing by a digital data processor.

30. A method for updating an adaptive algorithm for processing data, comprising the steps of:

a) processing a data sequence in accordance with the adaptive algorithm to produce a processed data sequence;

b) filtering the data sequence to generate a filtered data term for the adaptive algorithm;

c) filtering an error term for the adaptive algorithm generated from at least the processed data sequence, each of said filtering steps using a similar or identical set of filter characteristics; and

d) updating the adaptive algorithm in response to said filtered data term and said filtered error term.

31. The method of Claim 30, wherein each of said filtering steps uses an identical set of filter characteristics.

32. The method of Claim 30, wherein said filtering step c) comprises convolving the processed data sequence with a first filter comprising said set of filter characteristics to generate a filtered processed data sequence.

33. The method of Claim 32, wherein said filtering step c) further comprises determining a difference between the filtered processed data sequence and an ideal filtered processed data sequence to produce said filtered error term.

34. The method of Claim 33, further comprising (i) detecting a sequence of said processed data sequence, and (ii) convolving said detected processed data sequence with a second filter comprising said set of filter characteristics to generate said ideal filtered processed data sequence.

35. The method of Claim 30, wherein said filtering step c) comprises determining a difference between the processed data sequence and an ideal processed data sequence to produce an error term.

36. The method of Claim 35, wherein said filtering step c) further comprises convolving the error term with a filter comprising said set of filter characteristics to generate said filtered error term.

37. The method of Claim 35, further comprising (i) detecting a sequence of said processed data sequence, and (ii) convolving said sequence-detected processed data sequence with a filter comprising said set of filter characteristics to generate said ideal filtered processed data sequence.

38. The method of Claim 30, wherein each of said first and second sets of filter characteristics comprises an error filter.

39. The method of Claim 38, wherein said filtering further comprises transposing a channel response to generate at least a subset of said set of filter characteristics.

40. The method of Claim 30, wherein said data sequence comprises a digital data signal.

41. The method of Claim 30, wherein said processing step a) comprises equalizing said data sequence, said processed data sequence comprises an equalized data signal, said filtered processed data sequence comprises a filtered equalized data signal, and said ideal filtered processed data sequence comprises an ideal filtered equalized data signal.

42. The method of Claim 30, wherein said set of filter characteristics is configured to minimize a dominant error type.

43. The method of Claim 42, wherein said dominant error type comprises a single bit error.

44. A computer-readable medium or waveform containing a set of instructions which, when executed by a signal processing device configured to execute computer-readable instructions, is configured to perform the method of claim 30.

45. The computer-readable medium or waveform of Claim 44, wherein said adaptive algorithm comprises an adaptive finite impulse response (FIR) algorithm.

46. The computer-readable medium or waveform of Claim 45, wherein said adaptive FIR algorithm comprises a least-mean-squares (LMS) gradient algorithm.

47. The computer-readable medium or waveform of claim 44, wherein said set of instructions comprises object code, source code and/or binary code.

48. The computer-readable medium or waveform of claim 44, wherein said set of instructions comprises digital code configured for processing by a digital data processor.

49. A signal processing architecture, comprising:
    a) an equalizer configured to equalize and/or filter a data sequence in accordance with an adaptive algorithm and provide an equalized data output;
    b) a first filter, configured to receive said data sequence and generate a filtered data term for said adaptive algorithm; and
    c) an error term circuit, configured to receive said equalized data output and provide a filtered error term for said adaptive algorithm, said error term circuit comprising a second filter having filter characteristics similar to said first filter.

50. The architecture of claim 49, wherein said equalizer comprises an adaptive finite impulse response (FIR) filter.

51. The architecture of claim 50, wherein said adaptive algorithm comprises a least-mean-square (LMS) algorithm.

52. The architecture of claim 49, wherein said error term circuit further comprises a signal processor configured to receive said equalized data output.

53. The architecture of claim 52, wherein said signal processor comprises a sequence detector configured to provide a sequence-detected equalized data output.

54. The architecture of claim 52, wherein said error term circuit further comprises a third filter configured to receive an output from said signal processor and provide an ideal equalized data output.

55. The architecture of claim 54, wherein said third filter comprises a target filter.

56. The architecture of Claim 54, said third filter comprising a portion structurally and/or functionally identical to said first and second filters.

57. The architecture of Claim 56, wherein said third filter further comprises a target filter.

58. The architecture of claim 52, further comprising a subtractor or comparator configured to (i) receive said equalized data output and an ideal equalized data output, and (ii) provide an error term.

59. The architecture of claim 58, wherein said subtractor or comparator comprises said subtractor, and said subtractor is further configured to subtract one of said equalized data output and said ideal equalized data output from the other of said equalized data output and said ideal equalized data output.

60. The architecture of claim 58, wherein said second filter receives said error term and provides said filtered error term.

61. The architecture of claim 52, wherein said second filter receives said equalized data output and provides a filtered equalized data output.

62. The architecture of claim 61, wherein said error term circuit further comprises a signal processor and a third filter configured to receive said equalized data output and provide an ideal equalized data output.

63. The architecture of claim 62, wherein said third filter comprises a target filter.

64. The architecture of claim 62, wherein said error term circuit further comprises a fourth filter configured to receive said ideal equalized data output and provide an ideal filtered equalized data output.

65. The architecture of claim 64, further comprising a subtractor or comparator configured to (i) receive said filtered equalized data output and said ideal filtered equalized data output, and (ii) provide said filtered error term.

66. The architecture of claim 65, wherein said subtractor or comparator comprises said subtractor, and said subtractor is further configured to subtract one of said filtered

equalized data output and said ideal filtered equalized data output from the other of said filtered equalized data output and said ideal filtered equalized data output.

67. The architecture of claim 49, wherein each of said first and second filters comprises an error filter.

68. The architecture of claim 67, wherein each of said first and second filters further comprises a matched filter.

69. The architecture of claim 67, wherein said error filter is configured to minimize one or more dominant error types.

70. The architecture of claim 69, wherein said one or more dominant error types comprise a single bit error event.

71. The architecture of claim 49, further comprising a receiver configured to receive data from a magnetic storage medium and provide said data sequence.

72. The architecture of claim 49, wherein said second filter is structurally and/or functionally identical to said first filter.

73. The architecture of claim 56, wherein said portion of said third filter is structurally and/or functionally identical to said first and second filters.

74. A signal processing architecture, comprising:

a) means for equalizing an input data signal in accordance with an adaptive algorithm, configured to produce an equalized data signal;

b) first means for filtering said input data signal, configured to generate a filtered data term for said adaptive algorithm; and

c) means for providing a filtered error term for said adaptive algorithm, configured to receive said equalized data signal and comprising a second means for filtering having filter characteristics similar to said first means for filtering.

75. The architecture of claim 74, wherein said means for equalizing comprises an adaptive finite impulse response (FIR) filter.

76. The architecture of claim 74, wherein said means for providing said filtered error term comprises a means for processing said equalized data signal.

77. The architecture of claim 76, wherein said means for processing comprises a sequence detector configured to provide a sequence-detected equalized data signal.

78. The architecture of claim 76, wherein said means for providing said filtered error term further comprises a third means for filtering an output from said means for processing, configured to provide an ideal equalized data signal.

79. The architecture of claim 78, wherein said third means for filtering comprises a target filter.

80. The architecture of Claim 78, said third means for filtering comprising a portion having filter characteristics similar to said first and second filters.

81. The architecture of Claim 80, wherein said third means for filtering further comprises a target filter.

82. The architecture of claim 76, further comprising a means for providing an error term, configured to receive said equalized data signal and an ideal equalized data signal.

83. The architecture of claim 82, wherein said means for providing said error term comprises a subtractor, configured to subtract one of said equalized data signal and said ideal equalized data signal from the other of said equalized data signal and said ideal equalized data signal.

84. The architecture of claim 83, wherein said second means for filtering receives said error term and provides said filtered error term.

85. The architecture of claim 76, wherein said second means for filtering receives said equalized data signal and provides a filtered equalized data signal.

86. The architecture of claim 85, wherein said means for providing said filtered error term further comprises a means for processing said equalized data signal.

87. The architecture of claim 86, wherein said means for providing said filtered error term further comprises a first means for convolving said processed equalized data signal with a target filter, configured to provide an ideal equalized data signal.

88. The architecture of claim 87, wherein said means for providing said filtered error term further comprises a third means for filtering said ideal equalized data signal, configured to provide an ideal filtered equalized data signal.

89. The architecture of claim 88, further comprising further comprising a means for generating said filtered error term, configured to receive said filtered equalized data signal and said ideal filtered equalized data signal.

90. The architecture of claim 80, wherein said means for generating comprises a subtractor, configured to subtract one of said filtered equalized data signal and said ideal filtered equalized data signal from the other of said filtered equalized data signal and said ideal filtered equalized data signal.

91. The architecture of claim 74, wherein each of said first and second means for filtering comprises an error filter.

92. The architecture of claim 91, wherein each of said first and second means for filtering further comprises a matched filter.

93. The architecture of claim 91, wherein said error filter is configured to minimize one or more dominant error types.

94. The architecture of claim 93, wherein said one or more dominant error types comprise a single bit error event.

95. The architecture of claim 74, wherein said second means for filtering is structurally and/or functionally identical to said first means for filtering.

96. The architecture of claim 80, wherein said portion of said third means for filtering is structurally and/or functionally identical to said first means for filtering and said second means for filtering.

97. A system for reading magnetically recorded data, comprising:

a) the architecture of claim 49; and

b) at least one receiver communicatively coupled to said architecture for receiving said first data sequence.

98. The system of claim 97, wherein said equalizer comprises an adaptive finite impulse response (FIR) filter.

99. The system of claim 98, wherein said algorithm comprises a least-mean-square (LMS) algorithm.

100. The system of claim 97, wherein said error term circuit further comprises a sequence detector configured to receive said equalized data output and provide a sequence-detected equalized data output.

101. The system of claim 100, wherein said error term circuit further comprises a third filter configured to receive an output from said signal processor and provide an ideal equalized data output.

102. The system of Claim 100, said third filter comprising a portion similar to said first and second filters.

103. The system of Claim 102, wherein said third filter further comprises a target filter.

104. The system of claim 101, further comprising a subtractor or comparator configured to (i) receive said equalized data output and an ideal equalized data output, and (ii) provide an error term.

105. The system of claim 104, wherein said second filter receives said error term and provides said filtered error term.

106. The system of claim 101, wherein said second filter receives said equalized data output and provides a filtered equalized data output.

107. The system of claim 106, wherein said error term circuit further comprises a fourth filter configured to receive said ideal equalized data output and provide an ideal filtered equalized data output.

108. The system of claim 107, further comprising a subtractor or comparator configured to (i) receive said filtered equalized data output and said ideal filtered equalized data output, and (ii) provide said filtered error term.

109. The system of claim 97, wherein each of said first and second filters comprises an error filter.

110. The system of claim 109, wherein each of said first and second filters further comprises a matched filter.

111. The system of claim 109, wherein said error filter is configured to minimize one or more dominant error types.

112. The system of claim 111, wherein said one or more dominant error types comprise a single bit error event.

113. The system of claim 97, wherein said second filter is structurally and/or functionally identical to said first filter.

114. The system of claim 101, wherein said portion of said third filter is structurally and/or functionally identical to said first and second filters.

115. A magnetic recording system, comprising:

a) the system of Claim 97; and

b) a magnetic storage device, communicatively coupled to said system.

116. The magnetic recording system of claim 115, wherein said magnetic storage device comprises a floppy disk, a CD-ROM, a magnetic tape or a hard disk drive.